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PAT. & TRADEMARK OFF.

What Is Claimed Is:

Sub B1

1. An apparatus for communication between a plurality of processor devices, comprising

a post office memory including a plurality of mailbox memories;

each of the mailbox memories being write accessible only by its owner processor device, and read-accessible by its owner and other the processor devices.

2. An apparatus as in claim 1, wherein:

the plurality of processors includes a transmitting processor and a receiving processor;

a signal line provides communication between the processors; and

a subroutine in the receiving processor, corresponding to the signal line, reads the mailbox memory of the transmitting processor.

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~~3.~~ An apparatus as in claim 2, wherein at least one of the processor devices is external to a chip, and the other processor devices are on the chip.

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~~4.~~ An apparatus as in claim ~~3~~, wherein at least two of the processor devices on the chip are streamlined signal processors, and one of the processor devices on the chip is a master microprocessor.

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~~5.~~ An apparatus as in claim 2, wherein the signal line is a trigger, and further comprising a vector register pointing to the subroutine.

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~~6.~~ An apparatus as in claim 2, wherein the signal line is an interrupt, and wherein the subroutine is an interrupt service routine addressed by the interrupt.

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Sub B2

7. An apparatus as in claim 5, wherein the plurality of processors comprises at least three processor devices, including at least two transmitting processors and at least one receiving processor, and a signal line between the receiving processor and each of the transmitting processors, further comprising:

(a) an OR gate producing a logical-OR of the signal lines; and

(b) a mailbox status register associated with the receiving processor, each of the signal lines setting a status of one of the transmitting processors in the mailbox status register.

8. An apparatus as in claim 5, having at least three processor devices, including at least two transmitting processors and at least one receiving processor, and a signal line between the receiving processor and each of the transmitting processors, further comprising:

(a) an OR gate producing a logical-OR of the signal lines;

(b) a mailbox status register associated with the receiving processor, each of the signal lines setting a status of one of the transmitting processors in the mailbox status register.

9. An apparatus as in claim 1, wherein the post office memory is a multi-port random access memory (RAM), and each of the mailbox memories is a predetermined area of the RAM;

each predetermined area of the RAM further comprising means for providing write-access for only one of the processor devices to the predetermined area of the RAM from one of the ports; and

means for providing read-access to the RAM for the processor devices from each port.

10. An apparatus as in claim 9, wherein the device is a 4-port RAM.

11. An apparatus as in claim 10, wherein the predetermined area of RAM is 8 bytes.

12. An apparatus as in claim 1, further comprising:

a plurality of ports corresponding to the plurality of processor devices; and

wherein each of the ~~post office~~ mailbox memories comprises,

a plurality of register blocks, each of the register blocks including,

storage for a predetermined number of data bits,

a single data-in bus connection,

a plurality of data-out bus connections, one data-out bus connection for each of the plurality of ports,

a plurality of read input lines, one read input line from each of the ports, and

a single write line, the write line coming from ~~the~~ a port corresponding to the owner processor device.

13. A method of communicating among a plurality of processor devices, including a transmitting processor and a receiving processor, utilizing a post office with a plurality of mailboxes, the method comprising the steps of:

writing information into a predetermined one of the mailboxes in the post office with a transmitting processor;

signaling a receiving processor with the transmitting processor;

determining in the receiving processor which of the processor devices signalled the receiving processor; and

reading the information in the predetermined mailbox with the receiving processor.

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14. The method of claim 13, further comprising the step of the receiving processor device acting on the information.

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15. The method of claim 13, wherein the writing step occurs via a first port which is reserved to the transmitting processor device.

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16. The method of claim 13, wherein the signalling step comprises the transmitting processor device issuing an interrupt to the receiving processor device.

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17. The method of claim 13, the determining step including the receiving processor device executing an interrupt subroutine corresponding to the interrupt, and the reading step being performed by the interrupt subroutine.

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18. The method of claim 17, further comprising the step of the transmitting processor device setting a status register indicating the transmitting processor device, and the determining step comprising the receiving processor device reading the status register to determine the transmitting processor device.

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19. The method of claim 13, wherein the signalling step comprises the transmitting processor device issuing a trigger to the receiving processor device.

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20. The method of claim 19, the determining step including executing a subroutine pointed at in a vector register corresponding to the trigger, and the reading step being performed by the subroutine.

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21. The method of claim 20, further comprising the step of the transmitting processor device setting a mailbox status register indicating the transmitting processor device, and the determining step comprising the receiving processor device reading the mailbox status register to determine the transmitting processor device.

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22. A method of bi-directional communication between at least two processor devices, utilizing a post office with a plurality of mailboxes, the method comprising the steps of:

writing information into a first mailbox in the post office RAM, and signaling a second processor device with a first processor device;

writing information into a second mailbox in the post office RAM, and signaling the first processor device with the second processor device;

determining in the second processor device which of the processor devices signalled it;

determining in the first processor device which of the processor devices signalled it;

reading the information in the first mailbox with the second processor device; and

reading the information in the second mailbox with the first processor device.

23. A post office RAM comprising:

a multi-port RAM, having a plurality of cells and a plurality of ports, any one of the RAM cells being read-accessible by the plurality of ports, and write-accessible by only one of the ports.